REMARKS

Summary of Office Action

Claims 1-7, 11, 12 and 16-19 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura (US Pub. No. 2001/0002829) in view of Youn (US Pat. No. 5,856,816).

Claims 8, 9 and 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Applicant's alleged admittance of prior art.

Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Gooding et al. (US Pat. No. 4,580,265).

Summary of Amendment

No claims have been amended at this time. Claims 1-9, 11, 12, 14-20 are pending for further consideration.

PTO Form 326

It is noted that the Office Action Summary form (PTO Form 326) was not properly filled out. In particular, the Office Action Summary does not indicate the disposition of the claims or the acceptance of the replacement drawings filed with the Request for Continued Examination (RCE). For purposes of response, Applicants considers the replacement drawings as being accepted and the disposition of the claims as summarized above in the "Summary of the Office Action" section.

All Claims Comply with §103

Claims 1-7, 11, 12 and 16-19 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura in view of Youn (US Pat. No. 5,856,816), claims 8, 9 and 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Applicant's alleged admittance of prior art, and claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Youn, and further in view of Gooding et al. These rejections are respectfully traversed for the following reasons.

As an initial matter, the rejections in the current outstanding Office Action are the same rejections made in the previous Office Action (i.e., Final Office Action, paper no. 20050608) with the exception of claims 16-19, which were added after the final Office Action. As the current Office Action merely repeats the rejections of the previous Office Action with claims 16-19 added into the rejection groupings, Applicants disagree that the previous arguments are "moot in view of the new ground(s) of rejection" as asserted in the present Office Action since all grounds of rejection are, in fact, the same as that of the final Office Action, at least with respect to previously pending claims 1-7, 11, and 12. Hence, Applicants hereby incorporate by reference all the previously presented arguments (Response of November 14, 2005) with the following additional comments.

***Nishimura* and *Youn* fail to teach or suggest claimed features.**

As explained in detail in the previous response to the final Office Action (Response of 11/14/05: p. 14, 1st full paragraph) and incorporated herein by reference, Nishimura does not

teach at least "a first data polarity inversion driver...inverting the polarity of the first set of data" and "a second data polarity inversion driver...inverting the polarity of the second set of data" where "the first set of data is odd-numbered bits in an input data and the second set of data is even-numbered bits in the input data" as recited in claim 1. Rather, Nishimura discloses a 4-port polarity inverting circuit. Nishimura's system divides the input data into 4 segments and sends each segment to their respective ports (10-1) to (10-4). As explained previously, each of these data segments includes both odd and even numbered bits because the data stream is partitioned in sequential order. In other words, first data polarity inversion unit 10-1 processes and inverts both odd and even numbered bits. Likewise, each of the second, third, and fourth data polarity inversion units (10-2) to (10-4) processes and inverts both odd and even numbered bits.

The Office alleges that this deficiency is overcome by Youn. Youn teaches dividing pixel data in half based on odd and even numbered bits (latches 25, 26) and these odd/even pixel data are sent to respective D/A converters (27, 28) to drive the pixels on the LCD panel. While Youn teaches that the reference voltages of the D/A converters (27, 28) are selected based on the line data stored in the latches (25, 26) and the line conversion logic 24 converts the voltage's polarity for inversion, Youn still fails to teach at least "a first data polarity inversion drive" and "a second data polarity inversion driver" as recited in claim 1. Accordingly, Youn further fails to teach or even suggest "a first data polarity inversion driver determining ***whether a first data transition has occurred in a first set of data***, and inverting the polarity of the first set of data ***in accordance with the determined result***" (emphasis added) and "a second data polarity inversion

driver ***determining whether a second data transition has occurred in a second set of data*** and inverting the polarity of the second set of data ***in accordance with the determined result***."

At best, Youn teaches a line conversion logic 24 that determines whether the reference voltage of one of the D/A converters (27, 28) should be inverted. However, there is no teaching or suggestion in Youn of at least "a first data polarity inversion driver determining whether a first data transition has occurred in a first set of data, and inverting the polarity of the first set of data in accordance with the determined result" and "a second data polarity inversion driver determining whether a second data transition has occurred in a second set of data and inverting the polarity of the second set of data in accordance with the determined result" as recited in claim 1.

Claim 11 recites, in part, "inputting the first and second sets of data to the first and second data polarity inversion driver...wherein the first set of data is odd-numbered bits of the input data and the second set of data is even-numbered bits of the input data." As explained above, Nishimura does not teach or suggest such a feature. Youn fails to teach or suggest "a first and second data polarity inversion driver" as explained above. Even if, *in arguendo*, the line conversion logic 24 is somehow construed as "a first and second data polarity inversion driver," Youn teaches that the odd/even pixel data are sent to the respective D/A converters 25, 26 and none of these signals are input to the line conversion logic 24. Accordingly, Youn further fails to teach or suggest at least the step of "inputting the first and second sets of data to the first and second data polarity inversion driver" as recited in claim 11.

Claim 16 recites, in part, "an odd data polarity inversion driver to generate a first inversion signal to invert odd-numbered input data bits when a first data transition is detected in the odd data" and "an even data polarity inversion driver to generate a second inversion signal to invert even-numbered input data bits when a second data transition is detected in the even data." Nishimura and Youn both fail to teach or suggest such a feature as explained above.

Therefore, Nishimura and Youn, whether taken individually or in combination, fail to teach or suggest each and every feature recited in independent claims 1, 11, and 16 for at least the reasons explained above.

***Nishimura* and *Youn* are not combinable.**

Applicants also reassert that Nishimura and Youn are not combinable in the manner asserted in the Office Action. As explained in detail in the previous response (Response of 11/14/05: p. 15) and incorporated herein by reference, Nishimura teaches dividing the input data into four sequential segments (i.e., each segment contains both odd and even numbered bits) and inputting each of these segments to their respective ports (10-1) to (10-4). Youn teaches dividing the pixel data in half as odd/even sets of data and none of odd/even pixel data are input to the line conversion logic 24. Given these two teachings, there is no motivation to incorporate Youn's odd/even division of pixel data into Nishimura's 4-port polarity inversion circuit as asserted in the Office Action.

The rationale given states that "it would have been obvious to one having ordinary skill in the art at the time of the invention to allow that the data be divided into even and odd groups as taught by Youn, to be used in a system similar to that which is taught by Nishimura, which

allows for 2-port data polarity inversion." First, Nishimura and Youn are ***not*** "similar" systems as explained above. Second, Youn does not teach a 2-port data polarity inversion as explained above. The rationale suggests that "by allow[ing] such a combination a large high-resolution liquid crystal display with a reduction in frequency EMI and power consumption." Nishimura teaches dividing the input data into 4 segments while Youn teaching dividing the pixel data into only 2 segments. Accordingly, it would appear that modifying Nishimura with Youn would ***increase*** the size of the data being processed and therefore have the ***opposite effect*** of the proffered rationale.

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For at least the reasons stated above, Nishimura and Youn, whether taken individually or in combination, fail to teach or suggest each and every feature recited in independent claims 1, 11, and 16. As to the dependent claims 2-7, 12 and 17-19, these claims all dependent from their respective independent claims 1, 11, and 16. Gooding and Applicants' alleged admitted prior art do not cure the deficiencies of the independent claims 1, 11, and 16. Hence, Applicants respectfully requests that the rejections to claims 1-7, 11, 12 and 16-19 be withdrawn.

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicant's undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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